

Subscribe (Full Service) Register (Limited Service, Free) Login

Search: © The ACM Digital Library O The Guide

US Patent & Trademark Office

SEARCH

Feedback Report a problem Satisfaction survey

A dynamic multithreading processor

Full text

慰Pdf (2.67 MB)

Source

International Symposium on Microarchitecture archive

Proceedings of the 31st annual ACM/IEEE international symposium on Microarchitecture

table of contents

Dallas, Texas, United States

Pages: 226 - 236 Year of Publication: 1998 ISBN:1-58113-016-3

Authors

Haitham Akkary Michael A. Driscoll

Sponsors

SIGMICRO: ACM Special Interest Group on Microarchitectural Research and Processing

IEEE-CS\TCMM: TC on Microprocessors & Microcomputers

Publisher IEEE Computer Society Press Los Alamitos, CA, USA

Additional Information: references citings index terms collaborative colleagues peer to peer

Tools and Actions:

Discussions Find similar Articles Review this Article

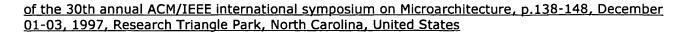
Save this Article to a Binder Display in BibTex Format

↑ REFERENCES

Note: OCR errors may be found in this Reference List extracted from the full text article. ACM has opted to expose the complete List rather than only correct and linked references.

- 1 J. E. Smith G. S. Sohi. The microarchitecture of Superscalar Processor. Procedeings of the IEEE, December 1995.
- 2 <u>Subbarao Palacharla</u>, <u>Norman P. Jouppi</u>, <u>J. E. Smith, Complexity-effective superscalar processors, Proceedings of the 24th annual international symposium on Computer architecture, p.206-218, June 01-04, 1997, Denver, Colorado, United States</u>
- 3 <u>Dean M. Tullsen</u>, <u>Susan J. Eggers</u>, <u>Henry M. Levy</u>, <u>Simultaneous multithreading: maximizing on-chip parallelism</u>, <u>Proceedings of the 22nd annual international symposium on Computer architecture</u>, <u>p.392-403</u>, <u>June 22-24</u>, <u>1995</u>, <u>S. Margherita Ligure</u>, <u>Italy</u>
- 4 Manoj Franklin, The multiscalar architecture, University of Wisconsin at Madison, Madison, WI, 1993
- 5 <u>Gurindar S. Sohi</u>, <u>Scott E. Breach</u>, <u>T. N. Vijaykumar</u>, <u>Multiscalar processors</u>, <u>Proceedings of the 22nd annual international symposium on Computer architecture</u>, <u>p.414-425</u>, <u>June 22-24</u>, <u>1995</u>, <u>S. Margherita Liqure</u>, <u>Italy</u>
- 6 Eric Rotenberg, Quinn Jacobson, Yiannakis Sazeides, Jim Smith, Trace processors, Proceedings

h c g c cf



- 7 <u>Pedro Marcuello</u>, <u>Antonio González</u>, <u>Jordi Tubella</u>, <u>Speculative multithreaded processors</u>, <u>Proceedings of the 12th international conference on Supercomputing</u>, p.77-84, <u>July 1998</u>, <u>Melbourne</u>, <u>Australia</u>
- 8 Mikko H. Lipasti , Christopher B. Wilkerson , John Paul Shen, Value locality and load value prediction, Proceedings of the seventh international conference on Architectural support for programming languages and operating systems, p.138-147, October 01-04, 1996, Cambridge, Massachusetts, United States
- 9 S. McFarling. Combining Branch Predictors. WRL Technical-Note TN-36, June 1993.
- 10 Avinash Sodani , Gurindar S. Sohi, Dynamic instruction reuse, Proceedings of the 24th annual international symposium on Computer architecture, p.194-205, June 01-04, 1997, Denver, Colorado, United States
- 11 H. Akkaary, A Dynamic Multithreading Processor, Ph.D. Dissertation, Department of Electrical and Computer Engineering, Portland State University, Technical Report PSU-ECE-199811 June 1998.
- 12 Manoj Franklin, Gurindar S. Sohi, ARB: A Hardware Mechanism for Dynamic Reordering of Memory References, IEEE Transactions on Computers, v.45 n.5, p.552-571, May 1996
- 13 J. Steffan, T. Mowry. The Potential for Using Thread-level Data Speculatition to Facilitate Automatic Parallelization, In Proceedings of HPC A-tV, pp. 2:-13, January: 1998:
- 14 S. Gopal, T. Vijayakumar, J. Smith, G. Sohi, Speculative Versioning Cache,. In Proceedings of HPCA-IV, pp. 195- 207, Jaauary 1998,
- 15 <u>Doug Burger</u>, Todd M. Austin, The SimpleScalar tool set, version 2.0, ACM SIGARCH Computer Architecture News, v.25 n.3, p.13-25, June 1997

↑ CITINGS 32

Haitham Akkary , Srikanth T. Srinivasan , Konrad Lai, Recycling waste: exploiting wrong-path execution to improve branch prediction, Proceedings of the 17th annual international conference on Supercomputing, June 23-26, 2003, San Francisco, CA, USA

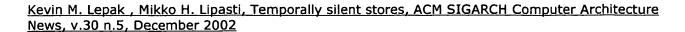
Amirali Baniasadi, Andreas Moshovos, Instruction distribution heuristics for quad-cluster, dynamically-scheduled, superscalar processors, Proceedings of the 33rd annual ACM/IEEE international symposium on Microarchitecture, p.337-347, December 2000, Monterey, California, United States

Antonia Zhai , Christopher B. Colohan , J. Gregory Steffan , Todd C. Mowry, Compiler optimization of scalar value communication between speculative threads, ACM SIGPLAN Notices, v.37 n.10, October 2002

<u>Jeffrey Oplinger</u>, <u>Monica S. Lam</u>, <u>Enhancing software reliability with speculative threads</u>, <u>ACM SIGPLAN Notices</u>, v.37 n.10, October 2002

Marcelo Cintra, José F. Martínez, Josep Torrellas, Architectural support for scalable speculative parallelization in shared-memory multiprocessors, ACM SIGARCH Computer Architecture News, v.28 n.2, p.13-24, May 2000

h c gc cf



<u>Il Park</u>, <u>Babak Falsafi</u>, <u>T. N. Vijaykumar</u>, <u>Implicitly-multithreaded processors</u>, <u>ACM SIGARCH Computer Architecture News</u>, <u>v.31 n.2</u>, <u>May 2003</u>

Milos Prvulovic, María Jesús Garzarán, Lawrence Rauchwerger, Josep Torrellas, Removing architectural bottlenecks to the scalability of speculative parallelization, ACM SIGARCH Computer Architecture News, v.29 n.2, p.204-215, May 2001

Karthik Sundaramoorthy, Zach Purser, Eric Rotenberg, Slipstream processors: improving both performance and fault tolerance, ACM SIGPLAN Notices, v.35 n.11, p.257-268, Nov. 2000

Gregory A. Muthler, David Crowe, Sanjay J. Patel, Steven S. Lumetta, Instruction fetch deferral using static slack, Proceedings of the 35th annual ACM/IEEE international symposium on Microarchitecture, November 18-22, 2002, Istanbul, Turkey

<u>Craig Zilles</u>, <u>Gurindar Sohi</u>, <u>Master/slave speculative parallelization</u>, <u>Proceedings of the 35th annual ACM/IEEE international symposium on Microarchitecture</u>, <u>November 18-22</u>, <u>2002</u>, <u>Istanbul</u>, <u>Turkey</u>

Youfeng Wu, Dong-Yuan Chen, Jesse Fang, Better exploration of region-level value locality with integrated computation reuse and value prediction, ACM SIGARCH Computer Architecture News, v.29 n.2, p.98-108, May 2001

Rajeev Balasubramonian, Sandhya Dwarkadas, David H. Albonesi, Dynamically allocating processor resources between nearby and distant ILP, ACM SIGARCH Computer Architecture News, v.29 n.2, p.26-37, May 2001

Karthik Sundaramoorthy, Zach Purser, Eric Rotenburg, Slipstream processors: improving both performance and fault tolerance, ACM SIGARCH Computer Architecture News, v.28 n.5, p.257-268, Dec. 2000

Quinn Jacobson, James E. Smith, Trace preconstruction, ACM SIGARCH Computer Architecture News, v.28 n.2, p.37-46, May 2000

<u>Pedro Marcuello</u>, <u>Antonio González</u>, <u>Clustered speculative multithreaded processors</u>, <u>Proceedings of the 13th international conference on Supercomputing</u>, p.365-372, <u>June 20-25</u>, 1999, <u>Rhodes</u>, <u>Greece</u>

Chen-Yong Cher, T. N. Vijaykumar, Skipper: a microarchitecture for exploiting control-flow independence, Proceedings of the 34th annual ACM/IEEE international symposium on Microarchitecture, December 01-05, 2001, Austin, Texas

Zach Purser, Karthik Sundaramoorthy, Eric Rotenberg, A study of slipstream processors, Proceedings of the 33rd annual ACM/IEEE international symposium on Microarchitecture, p.269-280, December 2000, Monterey, California, United States

Pedro Marcuello , Jordi Tubella , Antonio González, Value prediction for speculative multithreaded architectures, Proceedings of the 32nd annual ACM/IEEE international symposium on Microarchitecture, p.230-236, November 1999, Haifa, Israel

Anasua Bhowmik, Manoj Franklin, A fast approximate interprocedural analysis for speculative multithreading compilers, Proceedings of the 17th annual international conference on Supercomputing, June 23-26, 2003, San Francisco, CA, USA

Alvin R. Lebeck, Jinson Koppanalil, Tong Li, Jaidev Patwardhan, Eric Rotenberg, A large, fast

h c gc cf

instruction window for tolerating cache misses, ACM SIGARCH Computer Architecture News, v.30 n.2, May 2002

Artur Klauser, Dirk Grunwald, Instruction fetch mechanisms for multipath execution processors, Proceedings of the 32nd annual ACM/IEEE international symposium on Microarchitecture, p.38-47, November 1999, Haifa, Israel

J. Greggory Steffan, Christopher B. Colohan, Antonia Zhai, Todd C. Mowry, A scalable approach to thread-level speculation, ACM SIGARCH Computer Architecture News, v.28 n.2, p.1-12, May 2000

Chi-Keung Luk, Tolerating memory latency through software-controlled pre-execution in simultaneous multithreading processors, ACM SIGARCH Computer Architecture News, v.29 n.2, p.40-51, May 2001

Joshua A. Redstone, Susan J. Eggers, Henry M. Levy, An analysis of operating system behavior on a simultaneous multithreaded architecture, ACM SIGPLAN Notices, v.35 n.11, p.245-256, Nov. 2000

Rajeev Balasubramonian, Sandhya Dwarkadas, David H. Albonesi, Dynamically managing the communication-parallelism trade-off in future clustered processors, ACM SIGARCH Computer Architecture News, v.31 n.2, May 2003

Joshua A. Redstone, Susan J. Eggers, Henry M. Levy, An analysis of operating system behavior on a simultaneous multithreaded architecture, ACM SIGARCH Computer Architecture News, v.28 n.5, p.245-256, Dec. 2000

Theo Ungerer, Borut Robič, Jurij Šilc, A survey of processors with explicit multithreading, ACM Computing Surveys (CSUR), v.35 n.1, p.29-63, March 2003

Bing Luo, Chris Jesshope, Performance of a micro-threaded pipeline, Australian Computer Science Communications, v.24 n.3, p.83-90, January-February 2002

Eric Rotenberg , Jim Smith, Control independence in trace processors, Proceedings of the 32nd annual ACM/IEEE international symposium on Microarchitecture, p.4-15, November 1999, Haifa, Israel

Carlos Álvarez, Jesús Corbal, Esther Salamí, Mateo Valero, On the potential of tolerant region reuse for multimedia applications, Proceedings of the 15th international conference on Supercomputing, p.218-228, June 2001, Sorrento, Italy

Tong Liu, Shih-Lien Lu, Performance improvement with circuit-level speculation, Proceedings of the 33rd annual ACM/IEEE international symposium on Microarchitecture, p.348-355, December 2000, Monterey, California, United States

↑ INDEX TERMS

Primary Classification:

B. Hardware

B.8 Performance and Reliability

Additional Classification:

D. Software

• D.3 PROGRAMMING LANGUAGES

h c gc cf



Design, Management, Measurement

↑ Collaborative Colleagues:

Haitham Akkary: Michael Driscoll

Michael A. Driscoll Sébastien Hily Konrad Lai

Srikanth T. Srinivasan

Michael A. Driscoll: Haitham Akkary

W. Robert Daasch Douglas V. Hall

Chandana Sembakutti

- ↑ Peer to Peer Readers of this Article have also read:
 - Constructing reality

Proceedings of the 11th annual international conference on Systems documentation Douglas A. Powell , Norman R. Ball , Mansel W. Griffiths

<u>Data structures for quadtree approximation and compression</u>
 <u>Communications of the ACM</u> 28, 9

Hanan Samet

- A hierarchical single-key-lock access control using the Chinese remainder theorem
 Proceedings of the 1992 ACM/SIGAPP Symposium on Applied computing
 Kim S. Lee , Huizhu Lu , D. D. Fisher
- 3D representations for software visualization
 Proceedings of the 2003 ACM symposium on Software visualization
 Andrian Marcus , Louis Feng , Jonathan I. Maletic
- <u>Probabilistic surfaces: point based primitives to show surface uncertainty</u>
 <u>Proceedings of the conference on Visualization '02</u>
 Gevorg Grigoryan , Penny Rheingans

The ACM Portal is published by the Association for Computing Machinery. Copyright © 2004 ACM, Inc.

<u>Terms of Usage Privacy Policy Code of Ethics Contact Us</u>

Useful downloads: Adobe Acrobat QuickTime Windows Media Player Real Player